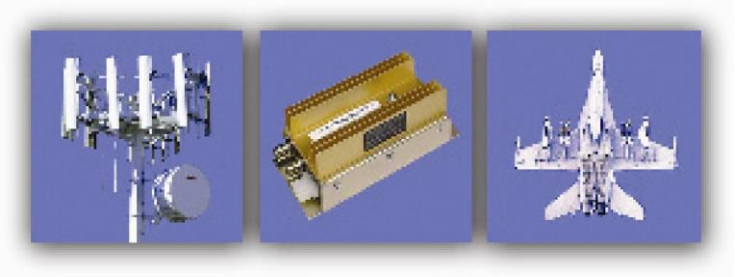
RF-60A & CER-10

General Processing Guidelines



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RF-60A & CER-10
General Processing Guidelines

Table of Contents

General Information

The RF-60A and Cer-10 products are part of the Taconic ORganic CERamic (ORCER) product line. With a dielectric constant of approximately 6.15 and 10, they are ideal high Dk products for applications requiring reduced circuit size and weight. The low electrical loss factor makes them an excellent selection for RF circuits.

It should be noted that the following processing recommendations are based on standard industry practices and optimal parameters may differ somewhat, depending on available processing equipment.

Material Properties					
	Dielectric Constant		Loss Tangent		Thickness Range
	10 GHz	1 MHz	10 GHz	1 MHz	
TLY	2.17 – 2.40		0.0009		0.0050" – 0.1870"
TLX	2.45 – 2.65		0.0019		0.0020" – 0.3750"
TLT		2.45 – 2.65		0.0006	0.0020" – 0.3750"
TLC	2.75-3.20		0.0030		0.0100" – 0.2500"
TLE	2.95-3.00		0.0028		0.0015" – 0.1250"
TSM-30	3.00		0.0015		0.0050" – 0.0600"
TLG	3.00-3.50		0.0038		0.0100" – 0.1200"
RF-30	3.00		0.0014		0.0100" – 0.1200"
RF-35	3.50	3.50	0.0028	0.0018	0.0100" – 0.1200"
RF-35A2	3.50		0.0018		0.0050" – 0.0600"
RF-35P	3.50	3.50	0.0035	0.0025	0.0020" – 0.1250"
RF-41	4.10		0.0038		0.0600" – 0.1250"
RF-43	4.30		0.0033		0.0100" – 0.1250"
RF-45	4.50		0.0037		0.0200" – 0.1250"
RF-60A	**6.15**		**0.0028**		**0.0100" – 0.1250"**
Cer-10	**10.0 (0.062 nominal)**		**0.0035**		**0.0040" – 0.1250"**

Table 1 – Material properties

Handling of PTFE Laminates

PTFE is a thermoplastic material which is very stable electrically and chemically when compared with common thermosetting resins such as epoxy, polyphenyleneoxide, polyimide and cyanate ester. Part of what gives PTFE its superior performance over frequency and temperature also makes the pure resin relatively soft. It is for this reason that all Taconic laminates are reinforced with glass fabric. The glass fabric reinforcement of the substrate greatly increases stability in the X and Y axis over non-woven or unreinforced PTFE products. While the glass fabric provides excellent

dimensional stability, the following process and handling precautions should be taken to prevent damage or deformation of the laminate during fabrication.

- **Do not mechanically scrub the material**

As with thin core or flexible substrates, mechanically scrubbing will stretch and deform the material. The pinch rollers used to secure the panel during scrubbing will also cause dents as particle or brush material are pressed into the surface of the laminate. Chemical cleaning is much preferred. Eliminating mechanical cleaning and unnecessary handling will improve the dimensional accuracy of subsequent processes by preventing mechanical distortion of the laminate.

- **Do not pick up a panel horizontally by one end or edge**

By allowing the material to flop over you may stretch the copper and substrate. Lift the panel by two parallel edges; preferably the two closest dimensionally.

- **Prevent contaminant deposits on the material or copper**

The use of clean protective gloves and slip sheets will prevent contamination and staining. You will not need to remove oils, grease or fingerprints if you don't deposit them.

- **Do not mechanically abrade the PTFE surface after etching/removing the copper**

If left undisturbed, the PTFE surface is very good for adhesion of solder mask, prepreg and bonding adhesive without further preparation. The etched surface of the PTFE is very wettable due to the rough tooth structure left behind after cooper removal. If the surface becomes disturbed, further surface preparation using sodium or plasma etching can improve wettability and adhesion to the surface.

- **Do not stack panels directly on top of each other**

Particles or debris on the surface of the panel can become imprinted into the copper and substrate of adjacent panels. The preferred method of storage is to rack the panels vertically. If panels must be stacked use clean, soft, slip sheet material between each panel and keep stack height to a minimum.

Drilling

Good hole quality can be achieved using Taconic recommended drill parameters. Standard 130° point geometry, PCB carbide drills work well with all Taconic PTFE-based laminates. Hole quality can be affected by drill sharpness. Taconic recommends using new drills for the best hole quality. Stack height should not exceed 2/3 the flute length of the smallest diameter drill being used. Standard phenolic entry material (≈ 0.020" [0.5mm] thickness) is acceptable along with aluminum / paper / aluminum entry. A hard phenolic backup board (≈ 0.090" to 0.125" [2.29mm – 3.18mm] thickness) is recommended to reduce bottom-side burring. The pressure of the drill foot should be a minimum of 40 psi and should be increased if topside burring is excessive.

The number of hits per drill will vary depending on the drill parameters, hole size, stack height, and laminate thickness. A worn drill bit usually results in an abnormally high number of nodules which may not be noticed until after plating. A normal hit count can range from 500 to 1500 hits for the RF-60A and Cer-10 materials.

All drilling debris must be removed prior to hole wall preparation such as plasma or sodium treatment. Thoroughly remove all debris in the holes with a high pressure air or water blast. If water is used, bake the laminate for 1 hour at 250^{o}F (121^{o}C) to remove moisture prior to through hole treatment.

Burring can occur if drilling conditions are not correct. If burring occurs, sanding is not recommended. Pumice scrubbing has been known to be effective, however Taconic does not recommend any process that may cause distortion of the laminate. The best solution to prevent burrs is by thoroughly understanding and implementing the optimum drilling process and parameters for your equipment.

Smearing is a condition where the PTFE resin has been heated to a point where it softens and is easily moved within the hole. It usually appears as a line between the copper foil and the plated copper. Assuming that sharp drill bits are being used, the solution is to reduce the speed (thus surface feet per minute) of the drill to prevent heat buildup. The chip load will increase so careful inspection for protrusions should be done after the electroless plating step, if possible. Protrusions may not be noticeable until after the electroless plating process, even if a high magnification microscope is used.

Hole wall tear-out, or gouging, is another possible defect caused during the drilling process. Gouging is usually an indicator of either a dull drill or an excessively high chip load. Another factor that can influence gouging is the fiberglass weave style. A coarse glass is more prone to gouging than a medium or fine glass style. RF-60A and Cer-10 use a fine weave glass and gouging should not be a problem. If gouging occurs, first check for worn drill bits before adjusting the drill parameters. If gouging persists, reduce the chip load. Care should be taken to keep drill bit temperatures to a minimum by keeping the surface feet per minute low while adjusting chip loads downward.

Inner Layer Preparation

Multilayer applications require that two or more laminates be bonded together to form a single circuit board. There are two important considerations when processing the circuit board. The first is registration of the features from one layer to another. The second is the condition of the bond surface prior to lamination.

Registration: Layer to layer registration is often a critical requirement of the finished circuit board and misregistration can cause a variety of issues such as open circuits and poor coupler performance. Therefore, it is important that the material be acclimated to the processing environment and the correct artwork compensation used. Acclimation to

the processing environment is simply making sure that the laminate is at ambient temperature prior to processing. It is recommended that if the laminate has seen extreme temperatures during shipment or storage, it should be placed in ambient conditions for 24 hours prior to processing.
All laminates experience movement after the copper foil has been etched. Various factors such as laminate thickness, glass style, construction, copper foil thickness, and circuit design contribute to the characteristic known as dimensional stability. The dimensional change data for various types of Taconic laminates are listed below. The data is for reference only and is dependent on the factors listed above. Most printed circuit board shops determine artwork compensation data by running samples or estimating based on previous experience.

Material Designation	Dimensional Change in Parts Per Million (PPM)
TLC	**200 – 400**
TLE	**220 – 400**
TLT	**400 – 600**
TLX	**400 – 600**
TLY	**400 - 800**
RF-30, RF-35, 35P	**200 – 400**
RF-60A	**400 – 600**
Cer-10	**400 – 600**

Table 2 – Dimensional change in parts per million

Bond Surface Condition: The condition of the substrate surface prior to bonding is critical in achieving good inner layer bond strength. As shown in Figure 2, the copper foil of the laminate has a dendrite structure designed to increase the copper peel strength. As the copper foil is etched, the dendrite imprint is left in the substrate surface. It is critical to subsequent multilayer bonding that this structure be present and undisturbed. Any mechanical abrasion of the substrate surface will destroy the imprint pattern and can result in poor bond strength between the layers. If the surface is destroyed, a sodium or plasma etch prior to multilayer bonding will greatly enhance surface adhesion. It is recommended that proper handling techniques be used at all times (see Handling of PTFE Laminates). It is also recommended that any processes used to clean the copper surface be chemical in nature, not mechanical.

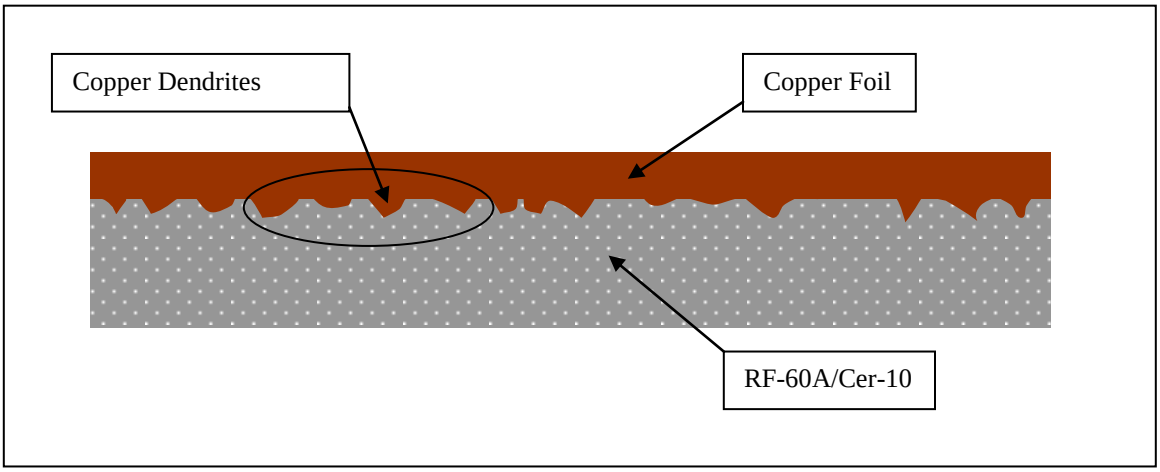

Figure 2 – Illustration of copper laminated to PTFE surface.

Hole Wall Preparation

PTFE based laminates require that drilled holes be subjected to a process which will prepare the PTFE resin system for subsequent plating. There are two processes that have been shown capable of providing void-free copper plating. One process is chemical in nature and involves a sodium-based solution that strips the fluorine atoms from the PTFE molecules. This process has been used for many years in the industry with great success. The advantages of sodium etching include long shelf life of the hole wall treatment, fast treatment time, and complete coverage. The primary disadvantage of sodium etchant is the volatility of the chemical. Various manufacturers and etchant services are available, call technical service for a complete list.
Another method of preparing the holes for plating is plasma etching. If the proper gases and cycles are used, plasma will allow plating to the PTFE resin. Experience has shown that the best gases to use are a mixture of hydrogen and nitrogen. Helium can also be used in many cases. The advantage of plasma etching is that it is a relatively safe procedure. Disadvantages include relatively long cycle times (35 to 60 minutes) and short shelf life of the effect (4 – 24 hours).

Sodium Treatment: A sodium-based chemical treatment process does an excellent job of preparing the PTFE through-hole surface prior to the plated through hole process. Follow the manufacturer's recommended treatment process. Bake for 1 hour at 250^{o}F (121^{o}C) prior to plating to remove moisture that may have been absorbed during the sodium treatment process. NOTE: Do not subject the treated holes to heavily concentrated chlorine-based chemical processes prior to electroless copper plating or direct metallization. Chlorine can have adverse effects on the sodium treatment and result in plating voids.

Plasma Etching: Plasma treat using a 30-70% Hydrogen, 70-30% Nitrogen gas mixture. Power setting for the RF-signal generator should be 60-75% of full rated power for 30-60 minutes depending on the hole diameter, number of holes, and thickness of

the board. Boards with relatively higher aspect ratios will require longer plasma cycle times. Industry experience has shown that gases such as helium and CF_4 are not as effective as hydrogen as evidenced by sporadic plating voids and higher contact angles.

Plating

After the hole wall has been properly prepared, PTFE-based laminates will accept either electroless copper or direct metallization plating. The electrolytic plating process is the same for PTFE or epoxy based materials. Typical plating consists of 1 – 1.5 mils (0.025mm – 0.038mm) of copper plate in the holes and/or on the surface.

Image, Develop, Etch, Strip

Prepare the copper surface, apply dry film, and image and develop using a standard process. The copper surface preparation should consist of microetching the copper. Scrubbing is not recommended for thin core PTFE-based materials or multilayer inner layers due to possible registration issues. Scrubbing can also destroy bonding surfaces and cause delamination of multilayers (see Inner Layer Preparation). If the surface is destroyed, a sodium or plasma etch prior to soldermask application or multilayer bonding will greatly enhance surface adhesion.

The etching process is the same as for a standard printed circuit board. Machine settings should be appropriate for the copper thickness of the multilayer inner layers. The substrate surface of the boards MUST NOT be touched or scrubbed. Strip the photoresist using a standard process.

Solder Mask

Soldermasking of PTFE materials can be achieved quite easily once the processes of cleaning, application and the adhesion mechanisms are thoroughly understood. The following covers these fundamentals.
Soldermask materials have changed drastically in the last 10 years with a move from two component fixed pot life epoxies, to single component heat cured epoxies, to the now standard liquid photo imageable soldermasks. The LPI's are different in that they incorporate a UV reactive component which allows these modified acrylic formulas (or combinations of epoxy and acrylates) to be imaged photographically for fine line resolution between fine pitch pads.

With the advantages of LPI's being their ease of use and resolution capability they often do not have the same adhesion characteristics as the previous pure epoxy systems. This fact must be taken into account when applying LPI's to PTFE laminates.

The mechanism for adhesion of soldermask (or prepreg or bonding film) to the PTFE laminate surface is the condition of the PTFE surface prior to application. By nature,

PTFE is a very low surface energy fluoropolymer and thus it has excellent non-stick properties, which make it highly popular in lubrication and release applications. However, the adhesion of the base copper cladding is achieved by lamination of the relatively rough (Table 3) treated copper surface to the PTFE material under high heat and pressure. This process is able to produce an excellent mechanical bond between the PTFE resin and the rough dendritic surface of the copper (Figure 2). It is the negative impression of the rough copper treatment that remains in the PTFE after etching the copper to form the circuitry pattern (Figure 3), which provides adequate surface area for mechanical bonding of the soldermask to the PTFE surface (Figure 4). Therefore it is important to eliminate traditional scrubbing techniques which may disturb or destroy this rough surface.

Copper Type	RzDin (microns) "Peak"	Ra (microns) "Average"
¼ oz. ED copper	4.95	0.80
½ oz. ED copper	6.65	1.00
1 oz. ED copper	9.60	1.50
2 oz. ED copper	9.70	1.55

Table 3 – Typical copper treatment roughness for various standard weights of electrodeposited copper foils.

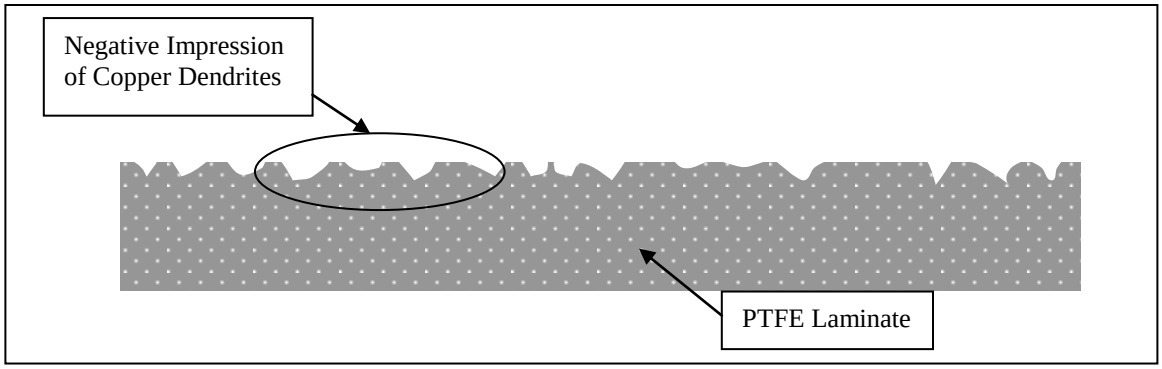

Figure 3 – Illustration of PTFE surface remaining after copper removal/etching.

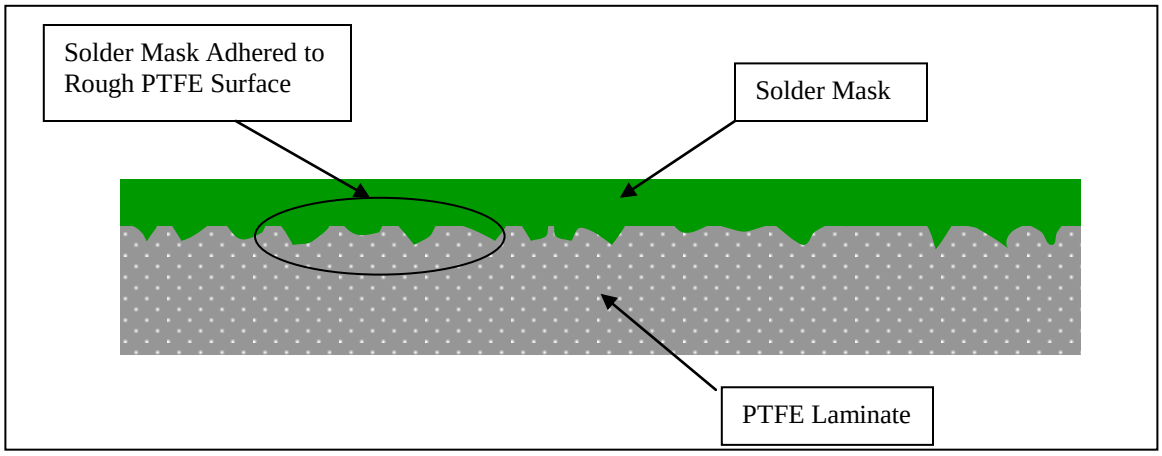

Figure 4 – Illustration of soldermask wetting and adhesion to rough PTFE surface.

With the need to replace the process a substitute process has been used which has several added benefits. Chemical cleaning of the copper surface offers the advantage of reduced mechanical stress on the material. This becomes critically important when dealing with thin laminates (≤0.010" or 25 mm) and or critical dimensional tolerances in soldermask or second stage drilling or routing. The removal of the scrubbing application also eliminates pits and dents which may be caused by high pressure contact with the steel or ceramic coated steel pinch rollers typically used in scrubbing machines to prevent panel movement during rotary scrubbing.

Soldermask Process – Pattern Plated Copper

1. Etch panels as normal to define circuitry pattern.
2. Allow plated metal etch resist (tin or tin/lead, in the case of nickel or gold surfaces obviously these will remain) to remain on panel through post etch inspection processes to prevent copper surface contamination, staining or oxidation prior to soldermask application.
3. Set up soldermask application process, prior to stripping or removing the metallic etch resist. *Note: For double sided soldermask applications, setup soldermask process to apply soldermask to the side of the panel with the largest copper area to be covered (i.e. if the ground plane is to be completely covered with soldermask then this would be the first side coated).*
4. Strip tin or tin/lead from copper surfaces. The copper surfaces should be bright and stain free following tin or tin/lead strip. *Note: Omit this process for nickel and gold finishes.*
5. Chemically clean and roughen the copper surfaces using an acid or alkaline cleaner followed by a micro-etch process which removes 30-60μ" of copper. This should provide adequate surface area for adhesion of soldermask to copper surfaces.
6. Dry panels thoroughly. If you do not have an adequate horizontal drier then an oven bake is recommended at 150-170°F (66-77°C) for 15-20 minutes. *Note: Drying process should not cause oxidation of copper surfaces. If oxidation occurs reduce drying time.*
7. Allow panels to cool to room temperature (approximately 5-10 minutes) and immediately apply soldermask.
8. Tack dry (LPI) or bake and cure (silk screened epoxy) soldermask per manufacturer's recommendation.
9. Continue processing per manufacturer's recommendation for LPI soldermasks (image, develop and cure).
10. For second side, repeat processes beginning with # 5.

Soldermask Process – Panel Plated Copper

1. Etch panels as normal to define circuitry pattern.
2. Strip dry film resist from panels and rinse and dry thoroughly to prevent copper surface oxidation.

3. Using clean white cotton gloves, perform post etch inspection immediately following dry film removal. Move panels to soldermask process directly after inspection.
4. Set up soldermask application process while post etch inspection is taking place to minimize hold time between etch, strip and soldermask application. *Note: For double sided soldermask applications, setup soldermask process to apply soldermask to the side of the panel with the largest copper area to be covered (i.e. if the ground plane is to be completely covered with soldermask then this would be the first side coated).*
5. Chemically clean and roughen the copper surfaces using an acid or alkaline cleaner followed by a micro-etch process which removes 30-60μ" of copper. This should provide adequate surface area for adhesion of soldermask to copper surfaces.
6. Dry panels thoroughly. If you do not have an adequate horizontal drier then an oven bake is recommended at 150-170°F (66-77°C) for 15-20 minutes. *Note: Drying process should not cause oxidation of copper surfaces. If oxidation occurs reduce drying time.*
7. Allow panels to cool to room temperature (approximately 5-10 minutes) and immediately apply soldermask.
8. Tack dry (LPI) or bake and cure (silk screened epoxy) soldermask per manufacturer's recommendation.
9. Continue processing per manufacturer's recommendation for LPI soldermasks (image, develop and cure).
10. For second side, repeat processes beginning with step # 5.

Solder Reflow

Hot air solder leveling is a common method of protecting exposed copper circuitry. Two basic types of hot air level machines are used in the industry, horizontal and vertical. By far the more popular of the two is the vertical machine. It is less expensive and easier to maintain than the horizontal type. However, the vertical machine subjects the printed circuit board to a more severe level of thermal shock than the horizontal. Once the board is clamped in the vertical machine, the only preheat the board sees is the few seconds above the solder pot prior to immersion. Typical immersion times are 5 – 6 seconds from entry into the solder pot to complete withdrawal. This minimal preheat time can be particularly harsh on PTFE based laminates due to their z axis expansion characteristics. When using hot air solder leveling on PTFE laminates, Taconic recommends a bake cycle of 2 – 3 hours at 300°F (149°C) just prior to the HASL process. The solder pot temperature should be maintained at 460° – 480°F (238° - 249°C) for optimal performance. Cycle time should be 5 – 6 seconds from the time of entry to the complete withdrawal of the board. Dwell time in the solder pot should not exceed 2 seconds.

Machining

Machining of PTFE-based substrates is typically more difficult than epoxy-based substrates due to the softness of the PTFE resin system. The style of fiberglass used in the substrate also affects the quality of routing with respect to burrs and fibers. The heavier the fiberglass weave, the more difficult it is to cut. Both RF-60A and Cer-10 use a fine fiberglass weave which routs well.

Taconic products can be successfully machined using standard router bits or end mills when the recommended methods and rout parameters are used. In addition to the rout parameters, an equally important factor in successful routing is having intimate contact throughout the routed package. Figure 5 shows a typical rout stack with phenolic entry and backer material on either side of the circuit board. Notice that the entry material rides on top of the copper traces leaving an air gap between the entry material and the PTFE substrate. In this case, the router bit will force the soft substrate into the air gap at the area circled in red. Many circuit board applications also have soldermask on top of the copper traces which increases the gap further. The solution to a cleaner cut is to introduce a material between the copper traces and the phenolic entry material that will conform at the edge and will help fill in the air gap. One type of paper that has been shown to work well is the paper found in between artwork film. It is thick enough to fill in the normal air gap and cuts without generating as much debris as other paper such as Kraft paper.

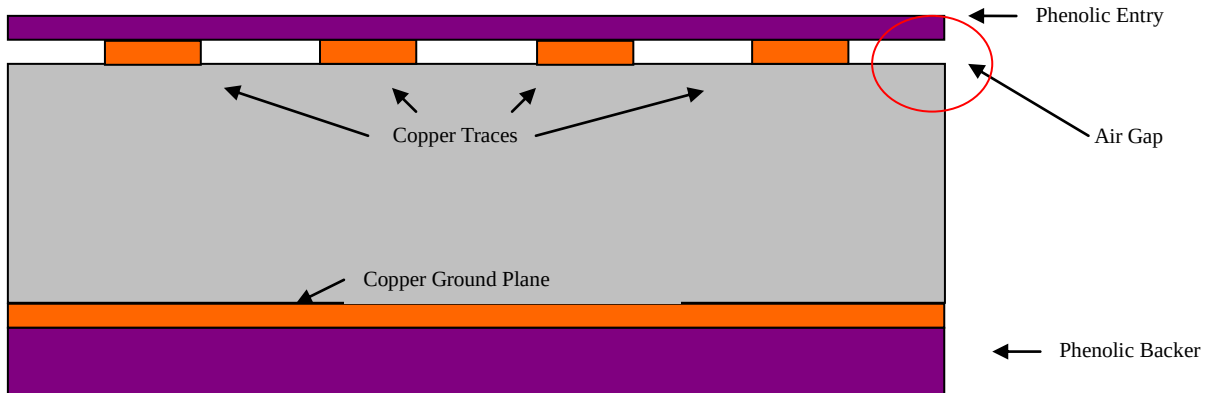

Figure 5 – A typical rout stack with phenolic entry and backer material on either side of the circuit board.

Recent routing trials using Taconic materials have yielded the following recommended rout parameters. These parameters are good starting points for all standard Taconic materials. Special materials such as those with heavy metal ground planes may require different rout parameters and are not addressed in this guideline.

Recommended Routing Parameters for All Taconic Materials							
		Spindle Type				z - Feed Rate	
		60,000 max		80,000 max			
Tool Diameter (mils)	**Chipload** (mils/rev)	**Spindle Speed** (rpm)	**Feed Rate** (in/min)	**Spindle Speed** (rpm)	**Feed Rate** (in/min)	**Without predrilling** (in/min)	**With predrilling** (in/min)
31.5	0.24	50000	11.8	50000	11.8	0.0	20
35.4	0.26	45000	11.8	45000	11.8	0.0	20
39.4	0.30	40000	11.8	40000	11.8	0.0	79
43.3	0.32	37000	11.8	37000	11.8	0.0	79
47.2	0.35	34000	11.8	34000	11.8	0.0	79
51.2	0.51	31000	15.8	31000	15.8	0.0	79
55.1	0.54	29000	15.8	29000	15.8	0.0	79
59.1	0.59	27000	15.8	27000	15.8	0.0	79
63	0.79	25000	19.7	25000	19.7	0.0	197
66.9	0.82	24000	19.7	24000	19.7	0.0	197
70.8	1.03	23000	23.6	23000	23.6	0.0	197
74.8	1.12	21000	23.6	21000	23.6	0.0	197
78.7	1.38	20000	27.6	20000	27.6	0.0	197
82.7	1.58	20000	31.5	20000	31.5	0.0	197
86.6	1.58	20000	31.5	20000	31.5	0.0	197
90.6	1.58	20000	31.5	20000	31.5	0.0	197
94.5	1.77	20000	35.4	20000	35.4	0.0	197
98.4	1.77	20000	35.4	20000	35.4	0.0	197
118.1	2.17	20000	43.3	20000	43.3	0.0	197
125	2.17	20000	43.3	20000	43.3	0.0	197

Table 4 – Recommended routing parameters for all Taconic materials

Recommended Routing Parameters for All Taconic Materials (metric)							
		Spindle Type				Z – Feed Rate	
		60,000 max		80,000 max			
Tool Diameter (mm)	**Chipload** (µm/rev)	**Spindle** Speed (rpm)	**Feed Rate** (m/min)	**Spindle Speed** (rpm)	**Feed Rate** (m/min)	**Without predrilling** (m/min)	**With predrilling** (m/min)
0.80	5	50000	0.25	50000	0.25	0	0.50
0.90	6	45000	0.27	45000	0.27	0	0.50
1.00	8	40000	0.32	40000	0.32	0	2.00
1.10	9	37000	0.33	37000	0.33	0	2.00
1.20	10	34000	0.34	34000	0.34	0	2.00
1.30	12	31000	0.37	31000	0.37	0	2.00
1.40	14	29000	0.41	29000	0.41	0	2.00
1.50	16	27000	0.43	27000	0.43	0	2.00
1.60	18	25000	0.45	25000	0.45	0	5.00
1.70	22	24000	0.53	24000	0.53	0	5.00
1.80	26	23000	0.60	23000	0.60	0	5.00
1.90	30	21000	0.63	21000	0.63	0	5.00
2.00	34	20000	0.68	20000	0.68	0	5.00
2.10	38	20000	0.76	20000	0.76	0	5.00
2.20	40	20000	0.80	20000	0.80	0	5.00
2.30	42	20000	0.84	20000	0.84	0	5.00
2.40	44	20000	0.88	20000	0.88	0	5.00
2.50	46	20000	0.92	20000	0.92	0	5.00
3.00	53	20000	1.06	20000	1.06	0	5.00
3.18	55	20000	1.10	20000	1.10	0	5.00

Table 5 – Recommended routing parameters for all Taconic materials (metric)

Multilayer

Print and etch inner layers using standard image/etch processes (see Inner Layer Preparation). Treat any copper surfaces with appropriate oxide or alternative processes. The PTFE surface of the laminate should not require further treatment if the surface is undisturbed after etching. Scrubbing is not recommended as it will distort the material and remove the mechanical tooth structure imparted by the laminated copper foil. It is this tooth structure which allows mechanical adhesion of the bond ply or prepreg. As mentioned earlier, RF-60A and Cer-10 type laminates can be laminated in a pure package or in a mixed package that typically uses an epoxy type laminate or prepreg. The choice of package depends on the electrical performance requirements of the package. Most mixed dielectric packages are designed with the digital or low frequency portion on the epoxy laminate and the high frequency on the fluoropolymer-based type laminate. When bonded together, this type of laminate reduces cost, space, connectors, and considerably shortens the distance the signal must travel.

A pure multilayer package of RF-60A and Cer-10 material can be bonded using Taconic's HT1.5 bonding film. This is a thermoplastic film with very low electrical loss and has been used in the industry for many years for bonding other types of PTFE based laminates. The HT1.5 bond film has a dielectric constant of 2.35 which is significantly different than the dielectric constants of the RF-60A (Dk 6.15) and Cer-10 (Dk 9.5-10.0) materials. However, the designer should be able to design with this in mind. HT 1.5 is a thermoplastic and will re-melt at approximately 400^{o} F (204^{o}C), therefore care must be taken when multiple or sequential lamination is required or when subjecting the board to thermal excursions such as Hot Air Solder Leveling.

Taconic also offers high performance, dielectric constant 3.0 to 3.5 and low loss TacPreg TPG prepregs. TPG prepregs are based on BT/epoxy/woven fiberglass/PTFE components. TPG prepregs can be laminated at conventional FR-4 temperatures 392^{o}F [200^{o}C].

Taconic recommends the following press cycle for TacPreg TPG prepregs:

- Vacuum Lamination Recommended
- Heat rise 3^{o}F - 10^{o}F / minute [1.5^{o}C – 5.5^{o}C] to 374^{o}F [190^{o}C] *
    - Flow window is 130^{o}F [80^{o}C] – 302^{o}F [150^{o}C]
- Maintain pressure at 73 psi [5 bar] until package reaches 100^{o}F [37^{o}C] then apply full pressure of 450 psi [31 bar]
- Hold (cure) for 1 hour
- Cool package under full pressure at < 6^{o}F [3^{o}C] / minute

Another bonding film used in the industry is FEP, a fluoropolymer-based film. The melt point of FEP is approximately 500^{o}F (260^{o}C) and offers greater protection from delamination when the board is subjected to post-lamination thermal cycles such as Hot Air Solder Leveling.

A mixed dielectric package consisting of RF type laminates and other laminates such as epoxy is not common, but can be accomplished quite easily. Bonding RF type laminates to an epoxy laminate is accomplished using standard epoxy prepreg. Since the high frequency RF signal does not see the epoxy due to the ground plane on the RF laminate, the higher loss of the epoxy prepreg does not come into play. Standard epoxy prepreg lamination cycles can be used per the manufacturer's recommendations. It is important that the RF type laminate is not scrubbed in case there are non-copper areas on the ground plane. The dendrite imprint left after etching the copper foil is critical to good bond strength and must not be disturbed prior to lamination.